IN THE CLAIMS

1(currently amended). An audio signal processor which modifies audio signal components not only in the conventional audio frequency band but also in the range of frequencies from about the upper limit of the conventional audio band to greater than 24kHz;

whereby the audio signal processor comprises a Delta Sigma Modulator (DSM ) that receives a non-interpolated digital audio signal sampled at a frequency of at least 198 kHz.

2(original). A processor according to claim 1, wherein the conventional audio band is about DC to about 20kHz.

3(original). A processor according to claim 1, wherein the conventional audio band is about 20 Hz to about 20 kHz.

4(previously presented). A processor according to claim 1, wherein the said range of frequencies extends to about 30kHz.

5(previously presented). A processor according to claim 1, wherein the said range of frequencies extends to about 50kHz.

6(previously presented). A processor according to claim 1, wherein the said range of frequencies extends to about 100kHz.

7(previously presented). A processor according to claim 1, wherein the said components are converted to n-bit digital signals where n is greater than one using a sampling rate greater than the Nyquist rate.

8(previously presented). A processor according to claim 1, wherein the said audio components are converted to 1-bit signals using a sampling rate in the range 198kHz to about 2.85MHz.

9(currently amended). A processor according to claim 8, wherein said DSM is a one bit DSM ~~the processor includes a 1-bit Delta Sigma Modulator (DSM)~~ for modifying the signal components.

10(original). A processor according to claim 9 wherein the said DSM is an nth- order (where n is greater than or equal to 1) Delta Sigma Modulator (DSM) having

an input for receiving a first 1-bit signal,

a quantizer for requantizing a p bit signal to 1-bit form the requantized signal being the output signal of the processor,

a plurality of signal combiners including

a first combiner for forming an integral of an additive combination of the product of the first signal and a first coefficient coefficient and of the product of the output signal and a second coefficient,

at least one intermediate combiner for forming an integral of an additive combination of the product of the first signal and a first coefficient and of the product of the second signal and the output signal and of the integral of the preceding stage, and

a final combiner for forming an additive combination of the product of the first signal and a first coefficient and of the integral of the preceding stage to form the said p bit signal which is requantized by the quantizer.

11(original). A processor according to claim 9 wherein the said DSM is an nth order (where n is greater than or equal to 1) Delta Sigma Modulator (DSM) having

a first input for receiving a first 1-bit signal, a second input for receiving a second 1-bit signal,

a quantizer for requantizing a p bit signal to 1-bit form the requantized signal being the output signal of the processor,

a plurality of signal combiners including

a first combiner for forming an integral of an additive combination of the product of the first signal and a first coefficient and of the product of the second signal and a second coefficient and of the product of the output signal and a third coefficient,

at least one intermediate combiner for forming an integral of an additive combination of the product of the first signal and a first coefficient and of the product of the second signal and a second coefficient and of the product of the output signal and a third coefficient and of the integral of the preceding stage, and

a final combiner for forming an additive combination of the product of the first signal and a first coefficient and of the product of the second signal and a second coefficient and of the integral of the preceding stage to form the said p bit signal which is requantized by the quantizer.

12(original). A processing according to claim 11, wherein the said first coefficients and the said second coefficients are chosen to combine the first and second signals in proportions defined by the first and second coefficients.

13(previously presented). A processor according to claim 11, wherein the third coefficients are chosen to provide noise shaping.

14(previously presented). A processor according to claim 10, wherein the first coefficient is variable.

15(previously presented). A processor according to claim 11, wherein the second coefficient is variable.

16(previously presented). A processor according to claim 14, further comprising means for generating the variable coefficient.

17(previously presented). A processor according to claim 11, wherein the first and second coefficients are fixed.

18(previously presented). A processor according to claim 11, comprising means for synchronising the bits of the first and second signals at the first and second inputs to a local clock which controls the clocking of the DSM.

19(previously presented). A processor according to claim 15, further comprising means for generating the variable coefficient.